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Tsukasa SHIRAISHI et al.:

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For: SEMICONDUCTOR DEVICE AND MODULE OF THE SAME

VERIFICATION OF ENGLISH TRANSLATION

Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

I, Takuji YAMADA , declare that I am conversant in both the Japanese and English languages and that the English translation as attached hereto is an accurate translation of Japanese Patent Application No. 09-250304 filed on September 16, 1997.

Signed this 26th day of October, 2005

Takuji Yamada

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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[DOCUMRNT NAME] SPECIFICATION

[TITLE OF THE INVENTION]

SEMICONDUCTOR DEVICE AND MODULE OF THE SAME

[CLAIMS]

[Claim 1] A semiconductor device comprising:

a multi-layer wiring board which comprises insulation layers made of resin-impregnated fiber sheets and circuit pattern layers laminated alternately and is provided with a three-dimensional wiring comprising said circuit pattern layers provided on both sides of the insulation layer and a plurality of inner via holes penetrating through each of said insulation layers and electrically connecting; and

at least first and second semiconductor elements mounted face down by flip chip bonding on the both side of the multi-layer wiring board wherein electrodes of said semiconductor elements are connected with each other by means of said three-dimensional wiring.

[Claim 2] The semiconductor device according to claim 1, wherein projections of one or more semiconductor elements mounted on either surface of said multi-layer wiring board in a direction perpendicular to said multi-layer wiring board

overlap with each other.

[Claim 3] The semiconductor device according to claim 1, comprising first, second and third semiconductor elements laminated via said multi-layer wiring board, wherein said multi-layer wiring board is bonded to cover said back surface of said second semiconductor element by bending said multi-layer wiring board whereon said first and said second semiconductor elements are mounted at specified positions on either side thereof, and said third semiconductor element is mounted by flip chip bonding, thereby to oppose said back surface of said second semiconductor element via said multi-layer wiring board.

[Claim 4] A module of a semiconductor device comprising:

said semiconductor device according to claim 1; and

a mother multi-layer wiring board having a circuit pattern formed on said surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are connected by electrical connection means.

[Claim 5] The module of the semiconductor device according to claim 4, wherein said electrical connection means is a projecting electrode which is interposed between said multi-layer wiring board of said semiconductor device and said mother multi-layer wiring board by bonding said back surface of said second semiconductor element onto said mother multi-layer wiring board thus placing said semiconductor device on said mother multi-layer wiring board, thereby to connect said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board.

[Claim 6] The module of the semiconductor device according to claim 4, wherein said electrical connection means establish electrical connection between said circuit pattern provided on said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board as said back surface of said second semiconductor element is bonded onto said mother multi-layer wiring board and said multi-layer wiring board of said semiconductor device mounted on said mother multi-layer wiring board is bent.

[Claim 7] The module of the semiconductor

device according to claim 4, wherein said electrical connection means is an electrically conductive supporting body which is electrically connected to said wiring in said multi-layer wiring board of said semiconductor device and is also used to fasten said semiconductor device onto said mother multi-layer wiring board, so as to establish electrical connection between said wiring of said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board by fastening said semiconductor device onto said mother multi-layer wiring board via said electrically conductive supporting body.

[Claim 8] The module of the semiconductor device according to claim 4, wherein said electrical connection means establish electrical connection between said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board as said semiconductor device is mounted on said mother multi-layer wiring board so that said multi-layer wiring board, which is bonded to cover said back surface of said second semiconductor element by bending said multi-layer wiring board whereon at least said first and said second semiconductor elements are

mounted at specified positions on either side thereof, makes contact with said mother multi-layer wiring board.

[Claim 9] A module of a semiconductor device comprising:

said semiconductor device according to claim 3; and

a mother multi-layer wiring board having a circuit pattern formed on said surface thereof, wherein

said circuit pattern provided on said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board are electrically connected to each other.

[DETAIL DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FIELD OF THE INVENTION]

The present invention relates to a semiconductor device formed by flip chip mounting semiconductor elements on both sides of a multi-layer wiring board having three-dimensional wiring which uses inner via holes.

[0002]

[PRIOR ART]

Attempts have been made to develop such a semiconductor element as a plurality of electronic circuits are incorporated in a single semiconductor element in order to make electronic apparatuses having semiconductor elements used therein more compact. In practice, however, it is difficult to make a single semiconductor element having all necessary functions due to limitations related to semiconductor material, production process, design rule and other factors, and it is often required to use a plurality of semiconductor elements. In such a case, in order to make the device smaller in size and run at a higher speed, chip-on-chip configuration is employed wherein the semiconductor elements are directly connected with each other by means of electrodes thereof as shown in Fig. 11. In the drawing, numeral 1 denotes a first semiconductor element, 2 denotes electrodes formed on the first semiconductor element 1, 3 denotes a second semiconductor element, 4 denotes electrodes formed on the second semiconductor elements, 10 denotes junctions made mainly of an electrically conductive metallic material such as solder, and 11 denotes a cured insulating resin. When such a chip-on-chip configuration is employed, length of wiring between the semiconductor elements can be made

shorter, transmission delay of electric signals is reduced, operation speed of the semiconductor device can be made faster and, because the semiconductor elements are mounted in laminated configuration, it is also made possible to make the semiconductor device smaller.

[0003]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

In case the first semiconductor element 1 and the second semiconductor element 3 are electrically connected via the junctions 10 in such a chip-on-chip configuration as described above, it is necessary to dispose the electrodes 2, 3 of the semiconductor elements to oppose each other. For this reason, general-purpose semiconductor elements cannot be used and it is required to use semiconductor elements which are designed by taking the positions of the electrodes 2, 3 into consideration, thus making it indispensable to design the semiconductor elements separately.

Also because the positions of the electrodes 2, 3 of the first and the second semiconductor elements are restricted, it becomes difficult to reduce the size of the semiconductor device in some cases, eventually resulting in lower production yield.

That is, an object of the present invention is

to provide a semiconductor device which is capable of operating at a higher speed and is smaller in size, by employing general-purpose semiconductor devices without using the chip-on-chip configuration.

[0004]

[MEANS FOR SOLVING PROBLEMS]

Therefore, the present inventors have intensively studied. As a result, they have found that it becomes possible to produce semiconductor devices of smaller size while maintaining a high operating speed of the semiconductor elements by mounting general-purpose semiconductor elements to oppose each other via a multi-layer wiring board on both sides of the multi-layer wiring board which has three-dimensional wiring employing inner via holes and connecting electrodes of the semiconductor elements with each other. Thus, the present invention has been completed.

[0005]

That is, the present invention provides a semiconductor device including: a multi-layer wiring board which includes insulation layers made of resin-impregnated fiber sheets and circuit pattern layers laminated alternately and is provided with a three-dimensional wiring having said circuit pattern

layers provided on both sides of the insulation layer and a plurality of inner via holes penetrating through each of said insulation layers and electrically connecting; and at least first and second semiconductor elements mounted face down by flip chip bonding on the both side of the multi-layer wiring board wherein electrodes of said semiconductor elements are connected with each other by means of said three-dimensional wiring.

The semiconductor device according to the present invention can be made smaller in size in a configuration similar to chip-on-chip configuration by employing the general-purpose semiconductor elements because the semiconductor elements are mounted face down by flip chip bonding via the multi-layer wiring board of thin layers. Particularly because the three-dimensional wiring employing the inner via holes is used in the multi-layer wiring board, the semiconductor elements mounted on both sides of the multi-layer wiring board can be connected by the three-dimensional wiring, thereby making it possible to make the wiring shorter compared to such a case where a conventional wiring board is used that lead wires are arranged to run over the substrate surface in two-dimensional wiring.

Consequently, according to the present invention, it becomes possible to achieve high operating speed of the elements by making the semiconductor device smaller in size and preventing the delay from occurring in electric signals with reduced wiring length, similarly to the case of employing the conventional chip-on-chip configuration even when the general-purpose semiconductor elements are used.

Also because the multi-layer wiring board is disposed between the semiconductor elements, the semiconductor element can be mounted or removed without causing a stress in the other semiconductor elements, thereby making it possible to prevent the semiconductor elements from being damaged.

[0006]

It is preferable that projections of one or more semiconductor elements mounted on either surface of the multi-layer wiring board in a direction perpendicular to the multi-layer wiring board overlap with each other.

When the semiconductor elements are mounted on the respective surfaces of the multi-layer wiring board so that projections thereof in a direction perpendicular to the multi-layer wiring board overlap

with each other, possibility of the multi-layer wiring board 107 to warp in the perpendicular direction (Z axis direction) can be reduced even in such a case as the insulating substrate constituting the multi-layer wiring board is made of a fiber sheet impregnated with a thermosetting resin which has a low rigidity and is liable to warp.

[0007]

The present invention also provides a semiconductor device including first, second and third semiconductor elements laminated via the multi-layer wiring board, wherein the multi-layer wiring board is bonded to cover the back surface of the second semiconductor element by bending the multi-layer wiring board whereon the first and the second semiconductor elements are mounted at specified positions on either side thereof, and the third semiconductor element is mounted by flip chip bonding, thereby to oppose the back surface of the second semiconductor element via the multi-layer wiring board.

When the multi-layer wiring board of thin layers is bent and the semiconductor device and the multi-layer wiring board are laminated alternately as described above, the semiconductor device can be

made small in size even when a large number of semiconductor elements are mounted.

[0008]

The present invention also provides a module for mounting semiconductor devices including the semiconductor device mounted on a mother multi-layer wiring board having a circuit pattern formed on the surface thereof with the semiconductor device and the mother multi-layer wiring board being connected by electrical connection means.

By mounting the semiconductor elements on the mother multi-layer wiring board, it becomes possible to form a high-density module, and it is also made possible to improve the productivity of the module by producing the semiconductor devices in advance and mounting only qualified semiconductor devices on the mother multi-layer wiring board after testing the semiconductor devices for the quality and reliability.

[0009]

The electrical connection means is preferably a projecting electrode which is interposed between the multi-layer wiring board of the semiconductor device and the mother multi-layer wiring board by bonding the back surface of the second semiconductor

element onto the mother multi-layer wiring board thus placing the semiconductor device on the mother multi-layer wiring board, thereby to connect the circuit pattern provided on the multi-layer wiring board and the circuit pattern provided on the mother multi-layer wiring board.

By using the projecting electrode for the electrical connection means, it becomes possible to form the connection means which utilizes the empty space between the multi-layer wiring board of the semiconductor device and the mother multi-layer wiring board, thereby making the module of the semiconductor device smaller in size.

[0010]

The electrical connection means preferably establish electrical connection between the circuit pattern provided on the multi-layer wiring board of the semiconductor device and the circuit pattern provided on the mother multi-layer wiring board as the back surface of the second semiconductor element is bonded onto the mother multi-layer wiring board and the multi-layer wiring board of the semiconductor device mounted on the mother multi-layer wiring board is bent.

By bending the multi-layer wiring board of the

semiconductor device and thereby forming the connection means, it becomes possible to reduce the number of electrode forming processes and thus reducing the production cost.

[0011]

The electrical connection means is preferably an electrically conductive supporting body which is electrically connected to the wiring in the multi-layer wiring board of the semiconductor device and is also used to fasten the semiconductor device onto the mother multi-layer wiring board, so as to establish electrical connection between the wiring of the multi-layer wiring board of the semiconductor device and the circuit pattern provided on the mother multi-layer wiring board by fastening the semiconductor device onto the mother multi-layer wiring board via the electrically conductive supporting body.

By using the semiconductor device having the electrically conductive supporting body such as metal which is electrically connected to the multi-layer wiring board, it becomes possible to handle the supporting body as if it is a pin of QFP and to mount the device onto the mother multi-layer wiring board or remove the device therefrom easily.

[0012]

The electrical connection means preferably establish electrical connection between the circuit pattern provided on the multi-layer wiring board and the circuit pattern provided on the mother multi-layer wiring board as the semiconductor device is mounted on the mother multi-layer wiring board so that the multi-layer wiring board, which is bonded to cover the back surface of the second semiconductor element by bending the multi-layer wiring board whereon at least the first and the second semiconductor elements are mounted at specified positions on either side thereof, makes contact with the mother multi-layer wiring board.

By using such connection means as described above, it becomes possible to make connection by using the lower region of the mounting surface of the semiconductor element and thereby to make the module of the semiconductor device smaller in size.

[0013]

The present invention also provides a module of the semiconductor device wherein alternate lamination of the semiconductor device and the multi-layer wiring board is mounted on the mother multi-layer wiring board which has a circuit pattern formed on the surface

thereof while the circuit pattern provided on the multi-layer wiring board of the semiconductor device and the circuit pattern provided on the mother multi-layer wiring board are electrically connected to each other.

By using such a module as described above, the semiconductor device can be mounted on the mother multi-layer wiring board with a high density.

[0014]

[EMBODIMENTS OF THE INVENTION]

Embodiment 1

Fig. 1 shows a semiconductor device according to the first embodiment of the present invention. This semiconductor device has two semiconductor elements on one side and one semiconductor element on the other side.

Fig. 1(a) is a perspective view of the semiconductor device and Fig. 1(b) is a cross sectional view taken along lines I-I' of the semiconductor device shown in Fig. 1(a). In the drawing, numeral 101 denotes a first semiconductor element, 102 denotes an electrode formed on an element forming surface of the semiconductor element 101, 103 denotes a second semiconductor element, 105 denotes a third semiconductor element, 104 and 106 denote electrodes

formed on the respective semiconductor elements, 107 denotes a multi-layer wiring board, 108 denotes a circuit pattern formed on the surface layer of the multi-layer wiring board, and 109 denotes inner via holes. Numeral 110 denotes junctions which provide electrical connection between the semiconductor elements 101, 103, 105 and the circuit pattern formed on the surface layer of the multi-layer wiring board 107, and 111 denotes an electrically insulating thermosetting resin.

[0015]

In the process of producing the semiconductor device shown in Fig. 1, first the three semiconductor elements 101, 103, 105 are prepared and ball bumps made of Au are formed on the surfaces of the electrodes 102, 104, 106 and then a required amount of an electrically conductive adhesive is applied onto the tips of the ball bumps. The electrically conductive adhesive is a mixture of a powder of electrically conductive metal such as Ag, Cu or Ni and a resin.

The semiconductor elements 101, 103 having the ball bumps made of Au or the like formed thereon with the electrically conductive adhesive applied thereto are mounted on the front surface of the multi-layer wiring board 107 and the semiconductor element 105

is mounted on the back surface of the multi-layer wiring board 107, each face down by flip chip bonding so that the semiconductor elements on both sides oppose each other via the multi-layer wiring board 107, with the adhesive cured by a heat treatment.

[0016]

Figs. 2(a), 2(b), and 2(e) show the layout of bumps provided on the back surfaces of the first semiconductor element 101, the second semiconductor element 103 and the third semiconductor element 105, and Figs. 2(c) and 2(d) show the circuit patterns formed on the top surface and the back surface of the multi-layer wiring board 107, respectively, whereon the semiconductor elements are mounted.

Bumps a1, a2, a3 and so on formed on the back surface of the first semiconductor element 101 and bumps b1, b2, b3 and so on formed on the back surface of the second semiconductor element 103 are connected to the electrodes x1, x2, x3 and so on, and the electrodes x11, x12, x13 and so on which are formed on the top surface of the multi-layer wiring board 107, respectively.

Bumps c1, c2, c3 and so on formed on the back surface of the third semiconductor element 105 are connected to the electrodes y1, y2, y3 and so on formed

on the bottom surface of the multi-layer wiring board 107.

The three-dimensional wiring of the multi-layer wiring board 107 establishes the electrical connection between the electrodes x1 and y1, between x2 and y2, between x3 and y3 and so on which are formed on the top and bottom surfaces of the multi-layer wiring board 107, respectively.

Consequently, as the first and the second semiconductor elements 101, 103 are mounted on one side and the third semiconductor element 105 is mounted on the other side of the multi-layer wiring board 107, the electrodes of the semiconductor elements are connected with each other by the three-dimensional wiring of the multi-layer wiring board 107, thus achieving a laminated construction similar to the conventional chip-on-chip configuration.

After the electrically conductive adhesive is cured, thereby to fasten the semiconductor elements 101, 103, 105 onto the multi-layer wiring board 107, the semiconductor elements are subjected to electrical tests to make sure of normal functions thereof.

[0017]

Then after filling the gap between the

semiconductor elements 101, 103, 105 and the multi-layer wiring board 107 with an insulating thermosetting resin 111, the insulating thermosetting resin 111 is completely cured by a heat treatment, thereby increasing the mechanical strength and quality of connection.

In case any of the semiconductor elements is found to be defective in the electrical test, only the defective semiconductor element is removed and replaced with a new semiconductor element. With this regard, bonding strength of the semiconductor elements is controlled to a minimum necessary level thereby to make it easy to remove the semiconductor element. Proper bonding strength per one bump for this purpose is about 3×10^6 to 30×10^6 N/m^2.

[0018]

The multi-layer wiring board 107 comprises insulating substrates made of resin-impregnated fiber sheets described in Japanese Patent Kokai Publication No. 6-268345 and circuit patterns laminated alternately, wherein the three-dimensional wiring is formed to connect the electrically conductive inner via holes formed through the insulating substrates and the circuit patterns.

Particularly, the insulating substrate of the

multi-layer wiring board 107 preferably consists of a fiber sheet made of glass fiber, aramid fiber or the like impregnated with a thermosetting resin. This is for the purpose of reducing the stress generated in the semiconductor elements to be mounted thereon and in the junctions by taking advantage of the Young's modulus of the resin-impregnated fiber sheet being lower than that of a wiring board which uses an inorganic material such as ceramics for the insulating substrate.

The material such as glass fiber and aramid fiber included in the substrate decreases the value of thermal expansion coefficient, which also contributes to the reduction of the stress generated in the semiconductor elements to be mounted thereon and in the junctions.

Use of the fiber sheet such as glass fiber and aramid fiber impregnated with the thermosetting resin for the insulating substrate of the multi-layer wiring board 107 reduces the stress generated in the semiconductor elements and in the junctions, thereby making it possible to produce high-quality semiconductor devices.

[0019]

Fig. 3 is a plan view of the semiconductor device

according to this embodiment viewed from the side of the first semiconductor element 101, wherein reference numerals identical to those of Fig. 1 denote the identical or corresponding portions.

As will be seen from Fig. 3, the projection of the semiconductor elements 101, 103 in the direction (hereinafter called Z axis direction) perpendicular to the wiring forming surface of the multi-layer wiring board 107 overlaps at least partially with the projection of the semiconductor element 105, which is mounted on the back surface, in the direction perpendicular to the wiring forming surface of the multi-layer wiring board 107. By disposing the semiconductor elements 101, 103, 105 in this configuration, the semiconductor device of the present invention becomes substantially symmetrical in Z-axis direction with respect to the multi-layer wiring board 107.

As the semiconductor elements are disposed substantially symmetrically in Z axis direction with respect to the multi-layer wiring board 107, the possibility of the insulating substrate of the multi-layer wiring board 107 to warp in the Z axis direction can be reduced even when the insulating substrate is made of the fiber sheet impregnated with

the thermosetting resin which has a low rigidity and is liable to warp.

Because the semiconductor device of the present invention can be made with less warping, it is made easier to mount the semiconductor device on the other wiring board and reduce the residual stress after mounting.

[0020]

According to this embodiment, as described above, electrical connection between the first and the second semiconductor elements 101, 103 and the third semiconductor element 105 is made by means of the multi-layer wiring board 107 and therefore it becomes possible to connect the elements with each other regardless of the positions of the electrodes formed on the semiconductor elements. Consequently, connection similar to that of chip-on-chip mounting can be made by using the general-purpose semiconductor elements without modification.

When compared to a case of connecting semiconductor elements by using a wiring board of the conventional configuration where inter-layer connection is made by forming the conventional through holes, use of the multi-layer wiring board 107 makes it possible to form three-dimensional wiring by means

of the inner via holes, increase the wiring density and increase the degree of freedom in the design of inter-layer connection, thus making it easier to run the lead wires. Thus because the use of the multi-layer wiring board 107 in wiring between similar semiconductor elements makes it possible to reduce the number of insulating layers to be laminated and to reduce the wiring length, the semiconductor device can be made smaller in size and it is advantageous in making the semiconductor device of shorter wiring length and higher operating speed.

Also because the semiconductor elements are not directly connected with each other, any of the semiconductor elements can be mounted or removed without causing damage to the other semiconductor elements, for example damage due to stress generated in the leads of the semiconductor elements.

Further because the semiconductor elements 101, 103, 105 are arranged in a substantially symmetrical configuration in the Z axis direction with respect to the multi-layer wiring board 107, the possibility of the multi-layer wiring board 107 to warp in the Z axis direction can be reduced even when the insulating substrate of the multi-layer wiring board 107 is made of the fiber sheet impregnated with the

thermosetting resin which has a low rigidity and is liable to warp.

Although the junctions 110 of the semiconductor elements are made from the Au ball bumps formed on the electrodes of the semiconductor elements and the electrically conductive adhesive in this embodiment, the bumps may also be formed by soldering or other process than wire bonding, and the bump may also be made of a conductive adhesive other than Au. And the electrically conductive adhesive may also be replaced with cream solder. The solder bump method named C4 process employed by Motorola Corp may be used. It is noted that the bump may be formed on the multi-layer wiring board 107, and an anisotropically conductive film (ACF) or the like may be used instead of the bump. In case an anisotropically conductive film is used, replacement of a defective semiconductor element is done by locally heating the anisotropically conductive film.

[0021]

Embodiment 2

Fig. 4 is a cross sectional view of a module of the semiconductor device according to the second embodiment of the present invention. In the drawing, reference numerals identical to those of Fig. 1 denote

the identical or corresponding portions. Numeral 112 denotes a mother wiring board whereon the semiconductor device is to be mounted, 113 denotes a circuit pattern formed in the surface layer of the mother wiring board, 114 denotes an Au wire for electrically connecting the multi-layer wiring board and the mother multi-layer wiring board.

The module according to this embodiment is produced in such processes as shown in Fig. 4, the semiconductor device comprising the multi-layer wiring board 107, whereon the semiconductor elements which have passed electrical tests are mounted, is fastened on the mother multi-layer wiring board 112 at a specified position by bonding the back surface of the third semiconductor element 105 onto the mother multi-layer wiring board 112 by means of an adhesive or the like, then the circuit pattern 108 on the front surface of the multi-layer wiring board 107 and the circuit pattern 113 on the front surface of the mother multi-layer wiring board 112 are connected with each other by the Au wire 114.

According to this embodiment, because the high-quality semiconductor device with less warp in the Z axis direction is mounted on the mother multi-layer wiring board, the semiconductor device

module of extremely high quality and high productivity can be produced.

Also because the semiconductor elements 101, 103, 105 mounted on the semiconductor device are made in such a configuration as laminated in the Z axis direction, surface area of the mother wiring board can be made smaller and the present invention can be applied to electronic apparatuses which are required to be smaller in size.

Although the Au wire 114 is used for the electrical connection means between the multi-layer wiring board 107 and the mother multi-layer wiring board 112 in Fig. 4, TAB (tape-automated bonding) or the like may also be used instead of the Au wire 114.

Particularly in this embodiment, because the multi-layer wiring board 107 and the mother wiring board 112 are made of the same material, physical constants such as thermal expansion coefficients of the two wiring boards are the same. Consequently, the stress generated in the third semiconductor element 105 which is interposed between both wiring boards is decreased and the quality of the module can be improved.

[0022]

Embodiment 3

Fig. 5 is a cross sectional view of a module of the semiconductor device according to the third embodiment of the present invention. In the drawing, reference numerals identical to those of Fig. 4 denote the identical or corresponding portions.

In the module according to this embodiment, the semiconductor device is mounted on the mother multi-layer wiring board 112 by a method similar to that of the second embodiment.

The multi-layer wiring board 107 which constitutes the semiconductor device has a thickness of about 200 μm, for example, and has a certain level of elasticity, thus it becomes possible to connect the multi-layer wiring board 107 directly to the mother wiring board by bending the multi-layer wiring board 107.

Therefore, as shown in Fig. 5, the multi-layer wiring board 107 of the semiconductor device mounted on the mother multi-layer wiring board 112 is bent and the circuit pattern provided on the multi-layer wiring board 107 and the circuit pattern provided on the mother multi-layer wiring board 112 are directly connected to each other, thereby establishing the electrical connection between both wiring boards and producing the module for the semiconductor device.

This process reduces the amount of connection material such as Au wire to be used and reduce the number of processes for producing the module, thereby making it possible to provide the module for the semiconductor device at a low cost with high productivity.

[0023]

Embodiment 4

Fig. 6 is a cross sectional view of a module of the semiconductor device according to the fourth embodiment of the present invention. In the drawing, reference numerals identical to those of Fig. 4 denote the identical or corresponding portions. Numeral 115 denotes an electrical junction such as bump electrode.

In the module according to this embodiment, the semiconductor device is mounted on the mother multi-layer wiring board 112 by a method similar to that of the second embodiment.

Protruding electrodes 115 as shown in Fig. 6 are used as the means for connecting the multi-layer wiring board 107 of the semiconductor device and the mother multi-layer wiring board 112. The protruding electrode 115 is made in a configuration similar to that of the junction 110 used in connecting the semiconductor element 101 or the like and the

multi-layer wiring board 107. That is, after forming the ball bumps made of Au on the circuit pattern of the mother multi-layer wiring board 112, a required amount of electrically conductive adhesive is applied to the tips of the bumps and the circuit pattern formed on the multi-layer wiring board 107 is placed thereon thereby electrically connecting the two wiring boards. In case some of the electrodes 102, 104 of the first semiconductor element 101 or the second semiconductor element 103 is exposed without being covered by the multi-layer wiring board 107, it may be connected with the junction layer 115 of the protruding electrode.

According to this embodiment, because the two wiring boards can be connected to each other by utilizing the narrow space between the semiconductor device and the mother multi-layer wiring board 112, the semiconductor devices can be mounted on the mother multi-layer wiring board 112 in a high density, thereby contributing to the size reduction of electronic apparatuses.

[0024]

Embodiment 5

Fig. 7 is a cross sectional view of a module of the semiconductor device according to the fifth embodiment of the present invention. In the drawing,

reference numerals identical to those of Fig. 4 denote the identical or corresponding portions. Numeral 116 denotes an electrically conductive supporting body.

In the module of the semiconductor device according to this embodiment, the semiconductor device is mounted on the mother multi-layer wiring board 112 by using the electrically conductive body 116 such as a metal frame which is electrically connected to the multi-layer wiring board 107 of the semiconductor device.

As shown in Fig. 7, electrical connection and mechanical fastening of the electrically conductive body 116 are made by holding the circuit pattern 108 of the multi-layer wiring board 107 at an edge of the multi-layer wiring board 107 and soldering or the like.

The semiconductor device is connected with the mother multi-layer wiring board 112 via the electrically conductive body 116.

According to this embodiment, it becomes possible to handle the semiconductor device equipped with the electrically conductive body 116 as if it is a QFP (quad flat module) and mount the semiconductor device on the mother multi-layer wiring board 112, thus making it easier to inspect and mount the semiconductor device and to replace the semiconductor

device in case of a failure.

[0025]

Embodiment 6

Fig. 8 is a cross sectional view of a module of the semiconductor device according to the sixth embodiment of the present invention. In the drawing, reference numerals identical to those of Fig. 4 denote the identical or corresponding portions.

In this embodiment, as shown in Fig. 8, the first semiconductor element 101 and the second semiconductor element 103 are mounted to oppose each other via the multi-layer wiring board 107, and the multi-layer wiring board 107 is bent to cover the back surface of the second semiconductor element and is bonded onto the back surface by means of an adhesive or the like.

The semiconductor device is mounted on the mother multi-layer wiring board 112 so that the circuit pattern formed on the multi-layer wiring board 107 is electrically connected to the circuit pattern formed on the mother multi-layer wiring board 112.

Since this configuration makes it unnecessary to provide particular means for electrically connecting the semiconductor device and the mother multi-layer wiring board 112, the amount of electrode

material and the number of producing processes can be reduced and, since the portion under the semiconductor device becomes the electrical connection means, surface area of the mother multi-layer wiring board 112 can be effectively utilized thereby making it possible to mount the semiconductor devices in a high density and contribute to the size reduction of electronic apparatuses.

[0026]

Embodiment 7

Fig. 9 is a cross sectional view of a semiconductor device according to the seventh embodiment of the present invention. In the drawing, reference numerals identical to those of Fig. 4 denote the identical or corresponding portions.

According to this embodiment, as shown in Fig. 9, the first semiconductor element 101 and the second semiconductor element 103 are mounted to oppose each other via the multi-layer wiring board 107 by flip chip bonding, while the multi-layer wiring board 107 is bent to cover the back surface of the second semiconductor element 103 and is bonded onto the back surface of the second semiconductor element 103 by means of an adhesive or the like. Then the third semiconductor element 105 is mounted by flip chip

bonding on the multi-layer wiring board 107 which is bonded to the back surface of the second semiconductor element 103 so that the third semiconductor element 105 and the second semiconductor element 103 oppose each other via the multi-layer wiring board 107.

In the semiconductor device of this embodiment, since the three semiconductor elements 101, 103, 105 are laminated by bending the multi-layer wiring board 107, packaging space can be effectively utilized thus making it possible to minimize the size of electronic apparatuses.

Although three semiconductor elements are laminated in this embodiment, the semiconductor elements can be mounted in larger number of levels by bending the multi-layer wiring board 107 furthermore.

[0027]

Embodiment 8

Fig. 10 is a cross sectional view of a module of the semiconductor device according to the eighth embodiment of the present invention. In the drawing, reference numerals identical to those of Fig. 4 denote the identical or corresponding portions.

According to this embodiment, as shown in Fig. 10, the semiconductor device mounted by lamination

using the multi-layer wiring board 107 which is bent over the first, second and third semiconductor elements according to the seventh embodiment is mounted on the mother multi-layer wiring board 112, while the multi-layer wiring board 107 and the mother multi-layer wiring board 112 are electrically connected with each other, thereby making the module.

Electrical connection between the multi-layer wiring board 107 and the mother multi-layer wiring board 112 is further made by directly connecting the circuit pattern formed on the multi-layer wiring board 107 bonded to cover the back surface of the third semiconductor element and the circuit pattern formed on the mother multi-layer wiring board 112.

According to this embodiment, since electrical connection is made by using the portion under the semiconductor device, packaging area of the mother multi-layer wiring board 112 can be effectively utilized, thereby making it possible to further improve the packaging efficiency because the semiconductor devices can be mounted in multiple layers. Thus it becomes possible to provide a module for semiconductor devices which is very advantageous for the size reduction of electronic apparatuses.

[0028]

[EFFECT OF THE INVENTION]

As will be clear from the above description, the semiconductor device according to the present invention has the semiconductor elements mounted to oppose each other via the multi-layer wiring board with the electrodes of the semiconductor elements being connected to each other by means of the three-dimensional wiring of the multi-layer wiring board, and therefore the elements can be connected with each other regardless of the arrangement of the electrodes of the semiconductor elements, thus making it possible to connect the general-purpose semiconductor elements without modification by a method similar to the chip-on-chip connection and provide the semiconductor device of smaller size and higher operating speed.

[0029]

According to the present invention, since the multi-layer wiring board is used instead of the conventional printed circuit board and connection between the semiconductor elements is made by using the three-dimensional wiring based on the inner via holes which makes it easier to run the lead wires, wiring length can be reduced, thereby preventing delays from occurring in the circuit response due to

the wiring length and the operating speed of the semiconductor device can be increased.

[0030]

Also because the semiconductor elements are not connected directly with each other, it becomes possible to remove or mount any of the semiconductor elements without causing damage to the other semiconductor elements.

[0031]

Also as the semiconductor device is mounted on the mother multi-layer wiring board, high-density packaging is made possible, thereby contributing to the size reduction of electronic apparatuses.

[BRIEF DESCRIPTION OF DRAWINGS]

[Fig. 1] Fig. 1(a) is a perspective view of the semiconductor device according to the first embodiment of the present invention, and Fig. 1(b) is a cross sectional view taken along lines I-I' of Fig. 1(a).

[Fig. 2] Fig. 2(a), 2(b), and 2(c) show the arrangement of the bumps formed on the semiconductor element according to the first embodiment of the present invention, and Fig. 2(c) and 2(d) show the circuit pattern of the multi-layer wiring board according to the first embodiment of the present

invention.

[Fig. 3] Fig. 3 is a top view of the semiconductor device according to the first embodiment of the present invention.

[Fig. 4] Fig. 4 is a cross sectional view of the module of the semiconductor device according to the second embodiment of the present invention.

[Fig. 5] Fig. 5 is a cross sectional view of the module of the semiconductor device according to the third embodiment of the present invention.

[Fig. 6] Fig. 6 is a cross sectional view of the module of the semiconductor device according to the fourth embodiment of the present invention.

[Fig. 7] Fig. 7 is a cross sectional view of the module of the semiconductor device according to the fifth embodiment of the present invention.

[Fig. 8] Fig. 8 is a cross sectional view of the module of the semiconductor device according to the sixth embodiment of the present invention.

[Fig. 9] Fig. 9 is a cross sectional view of the semiconductor device according to the seventh embodiment of the present invention.

[Fig. 10] Fig. 10 is a cross sectional view of the module of the semiconductor device according to the eighth embodiment of the present invention.

[Fig. 11] Fig. 11 is a cross sectional view of the semiconductor device of the chip-on-chip connection of the prior art.

[EXPLANATION OF KEYS]

1, 101...first semiconductor element

2, 102...electrode formed on the first semiconductor element

3, 103...second semiconductor element

4, 104...electrode formed on the second semiconductor element

5, 105...third semiconductor element

6, 106...electrode formed on the third semiconductor element

7, 107...multi-layer wiring board

8, 108...circuit pattern on the multi-layer wiring board

9, 109...inner via

10, 110 ,115...junction

11, 111...insulating board

12, 112...mother multi-layer wiring board

13, 113...circuit pattern on the mother multi-layer wiring board

114...Au wiring

116... electrically conductive supporting body

〔DOCUMENT NAME〕 DRAWINGS

Fig. 1

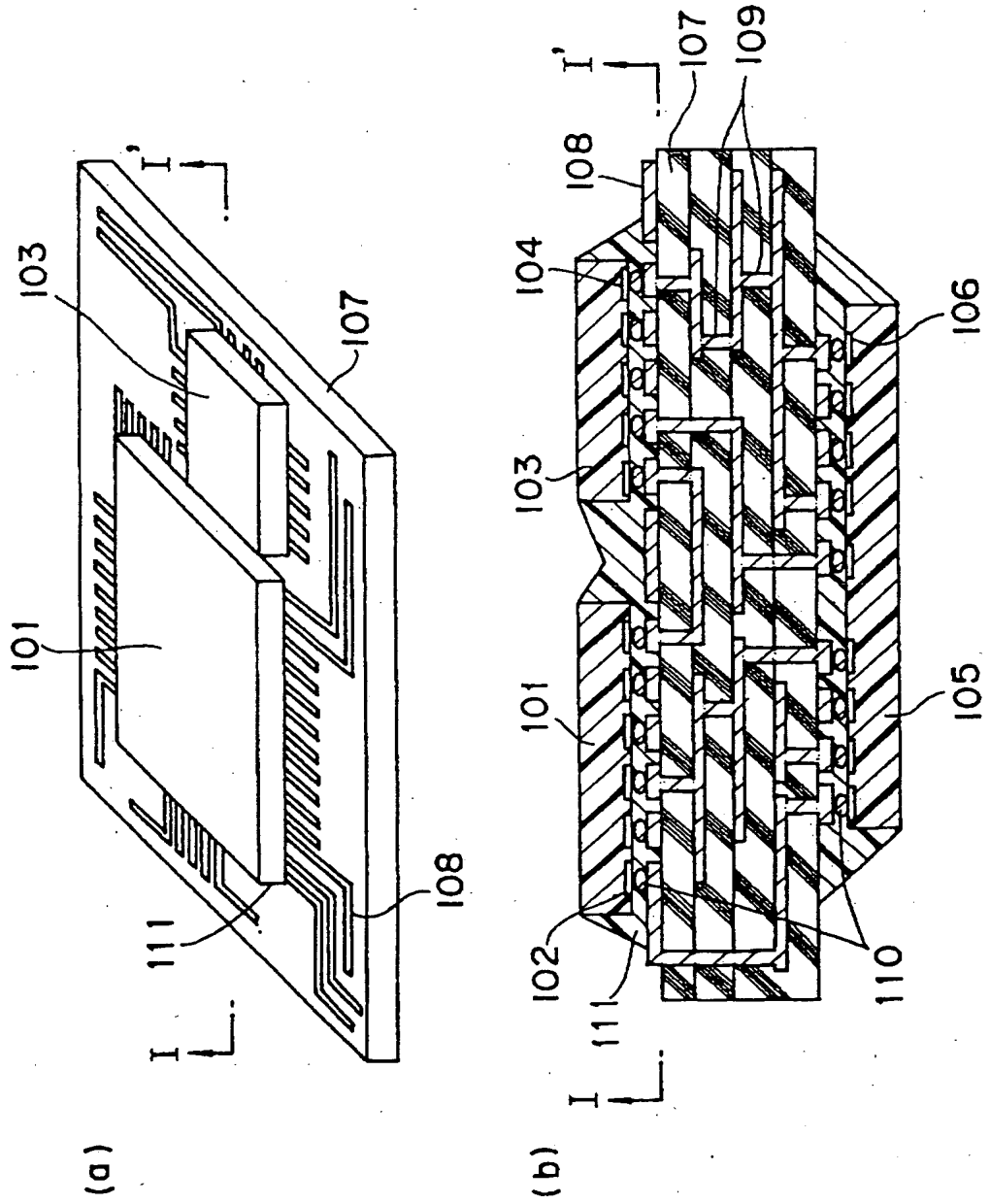


Fig. 2

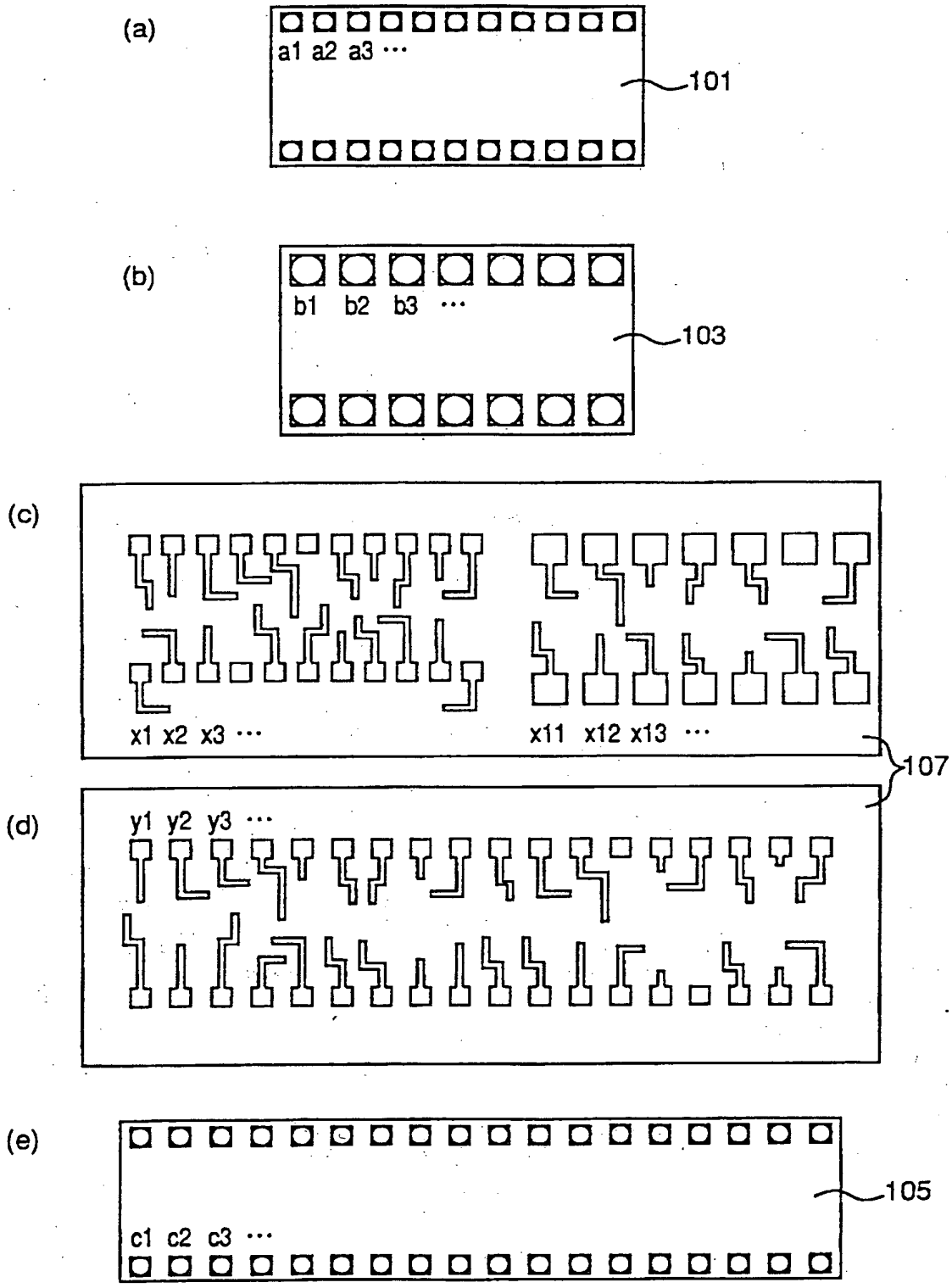

(a)
a1 a2 a3 ···
101
(b)
b1 b2 b3 ···
103
(c)
x1 x2 x3 ···
x11 x12 x13 ···
107
(d)
y1 y2 y3 ···
(e)
c1 c2 c3 ···
105

Fig. 3

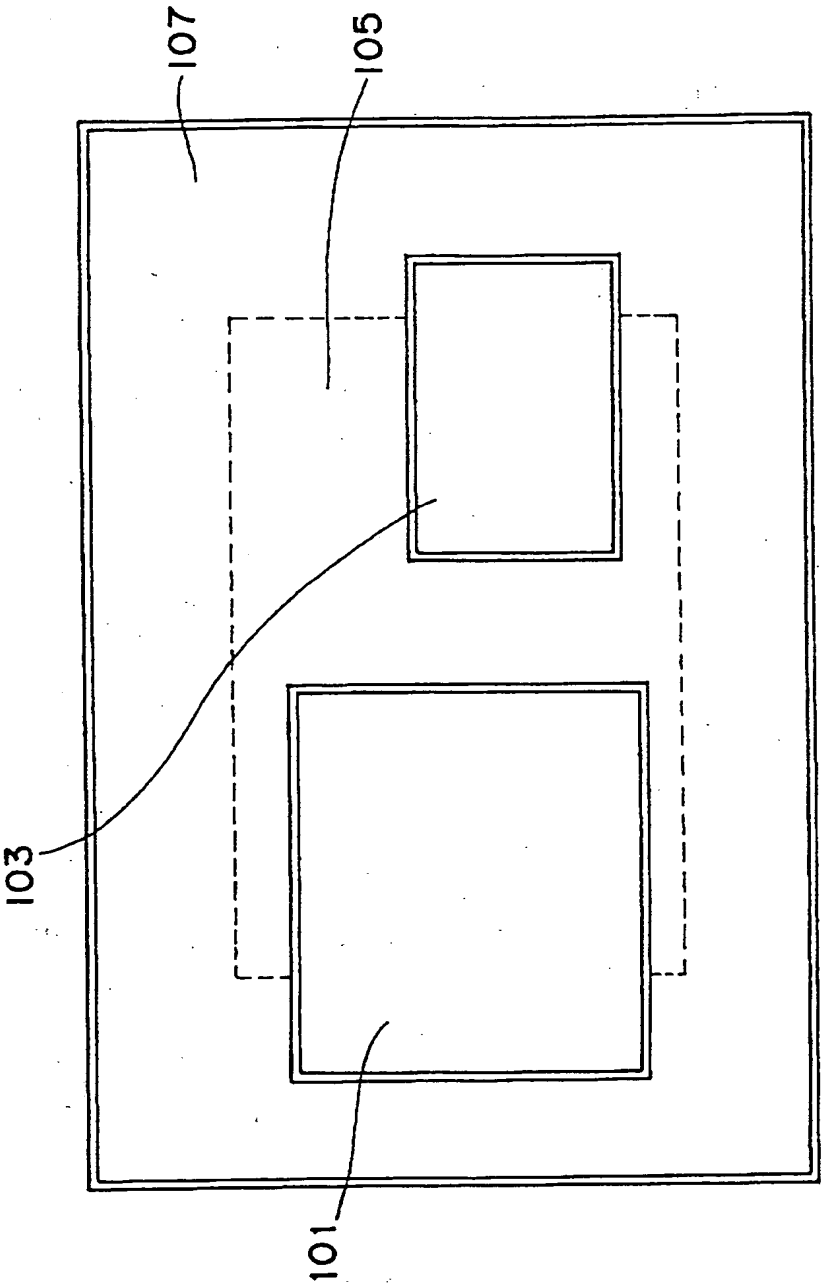


Fig. 4

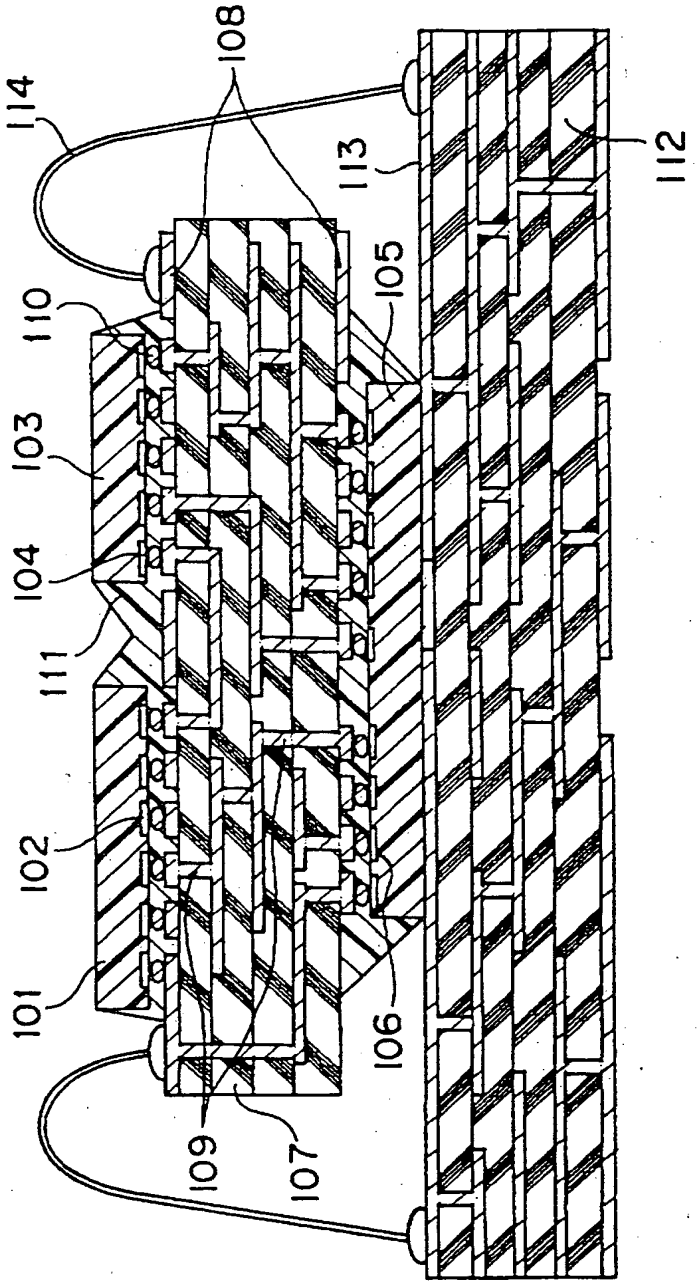


Fig. 5

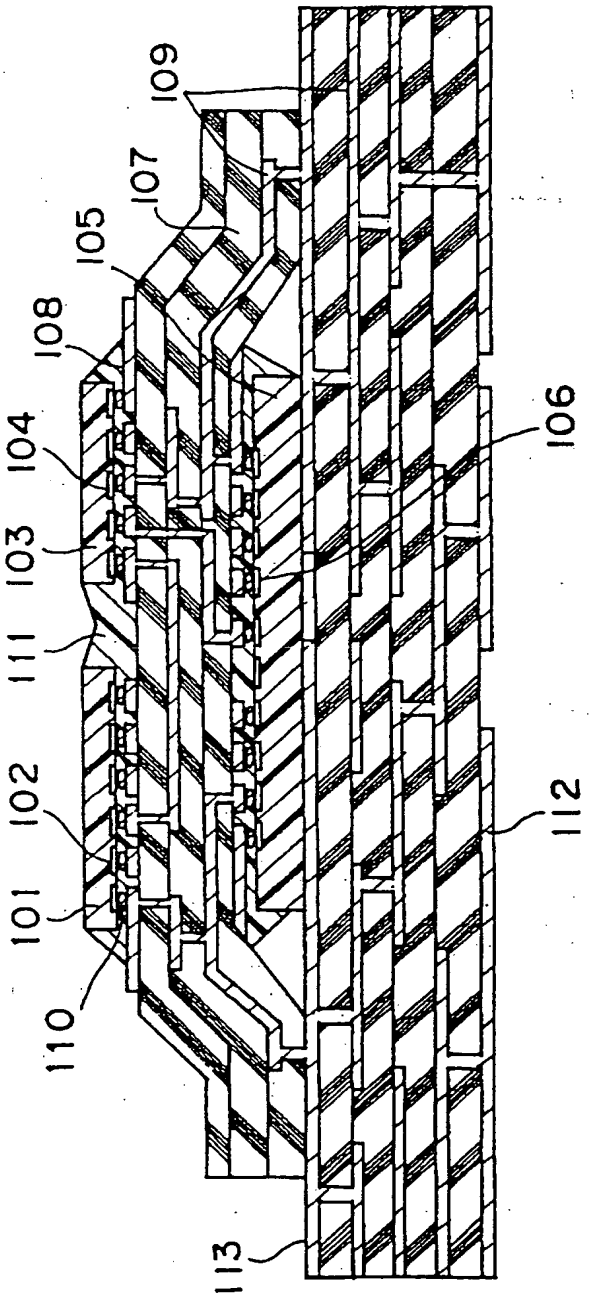


Fig. 6

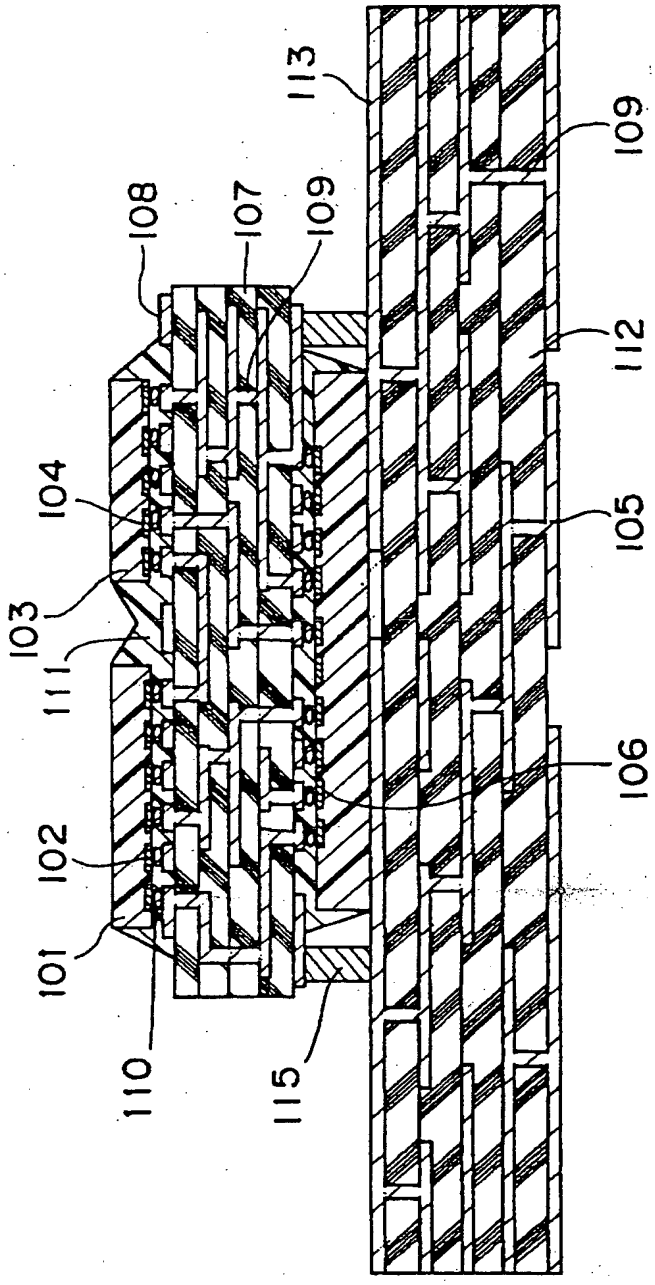


Fig. 7

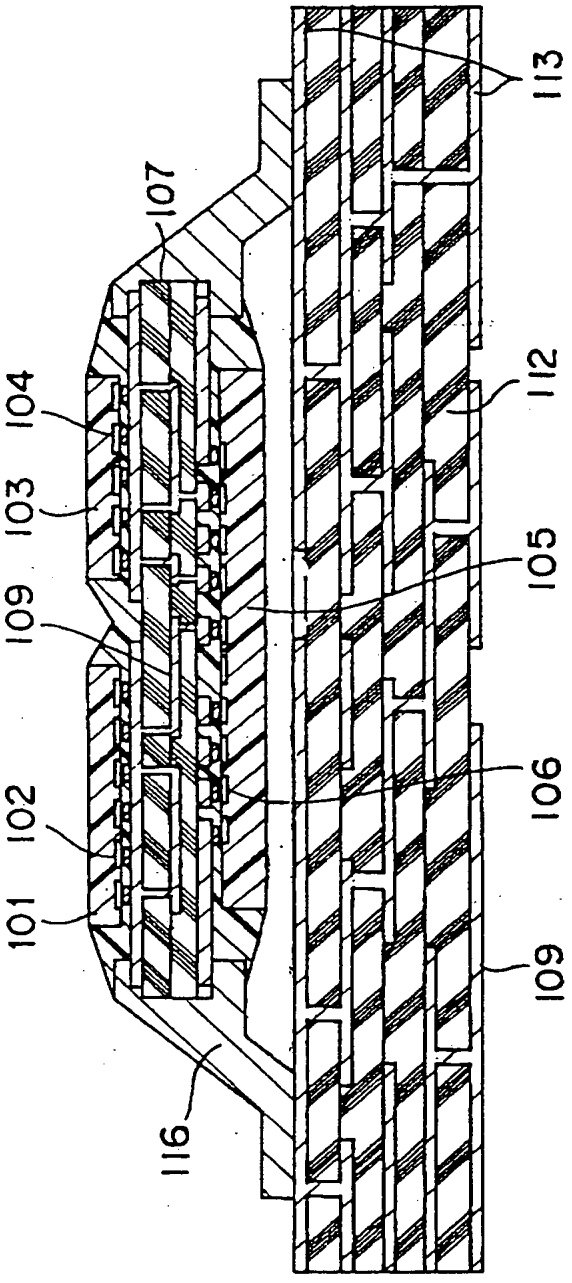


Fig. 8

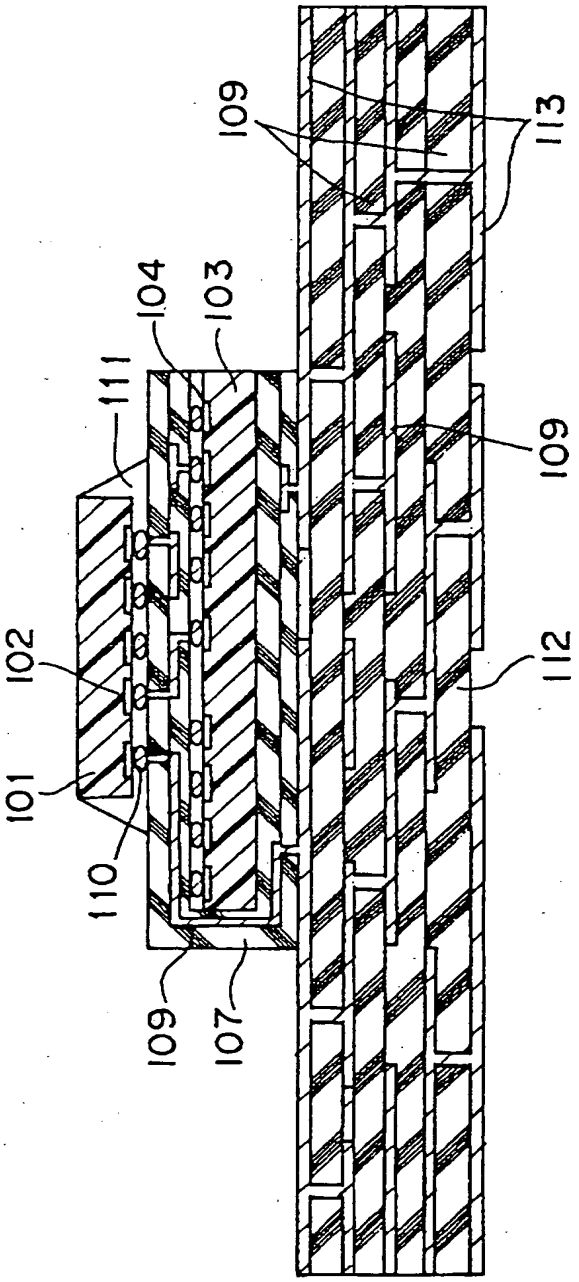


Fig. 9

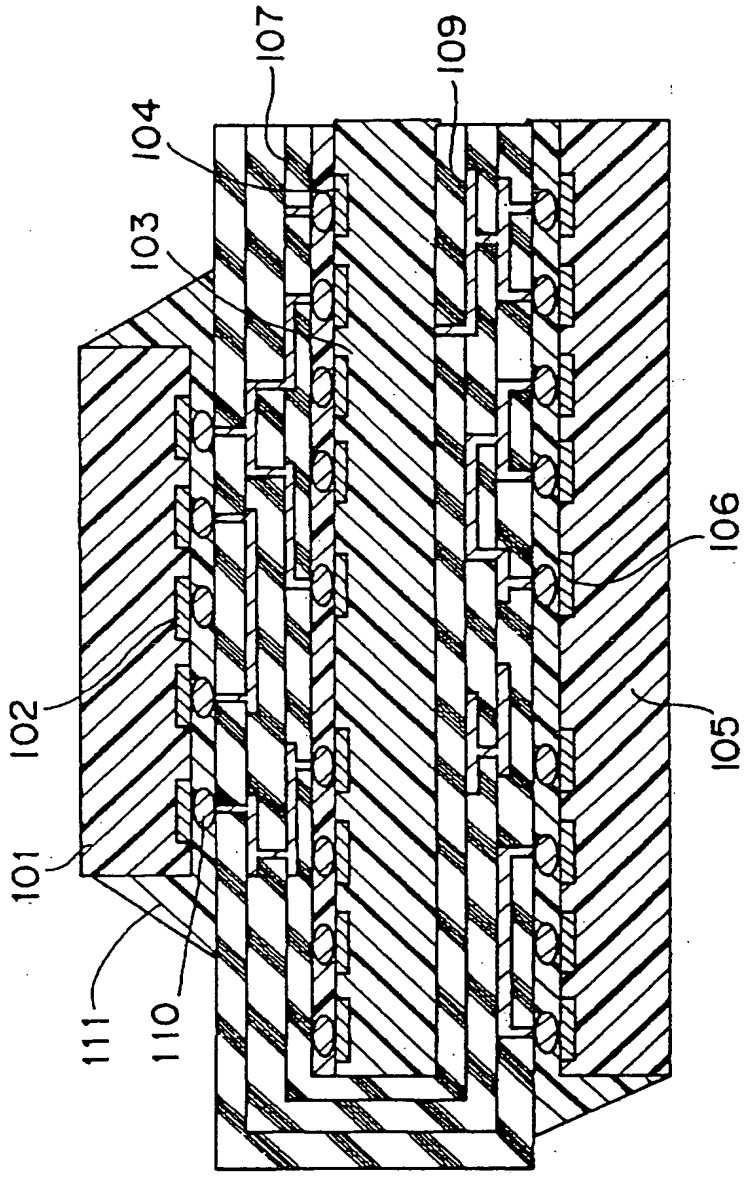


Fig. 10

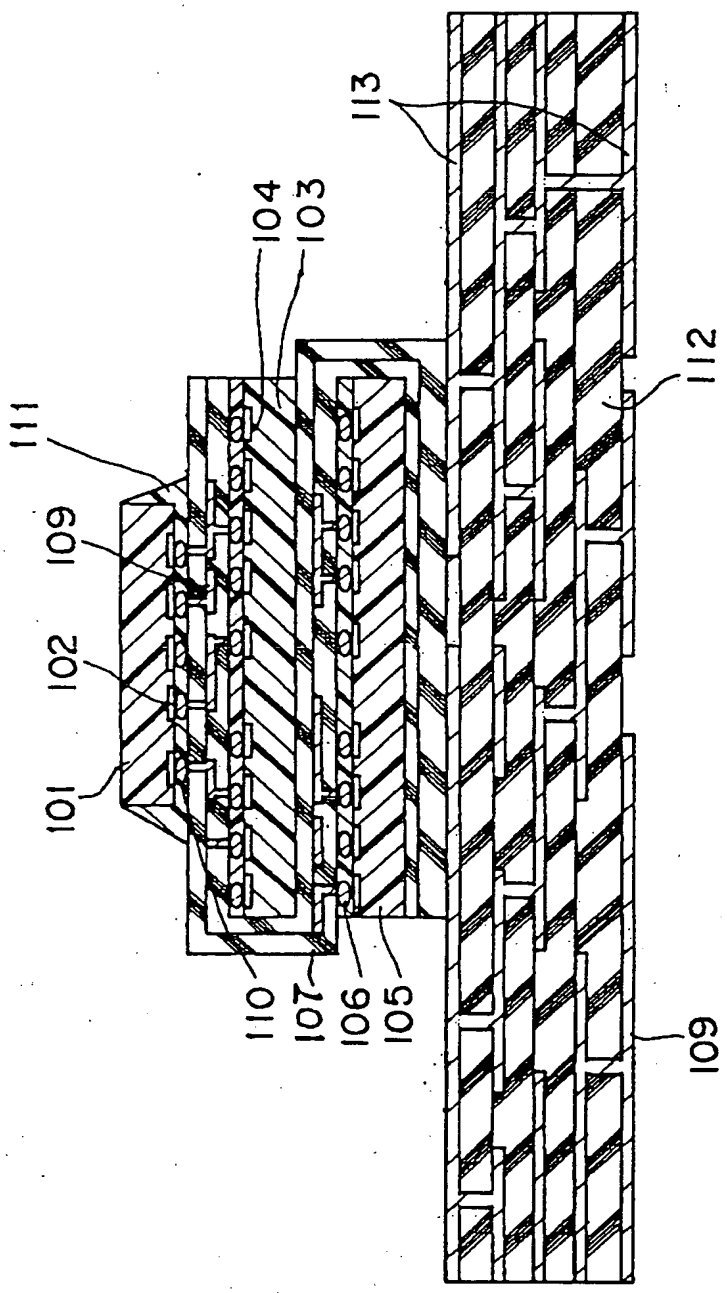
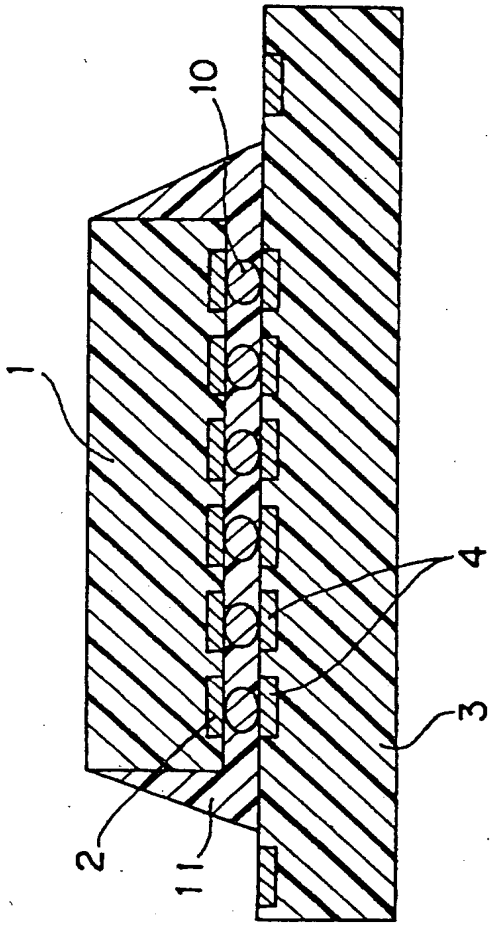


Fig. 11



[DOCUMENT NAME] ABSTRACT

[SUMMARY]

[PROBLEM] Providing a semiconductor device made by mounting semiconductor elements on both sides of a multi-layer wiring board having three-dimensional wiring which uses inner via holes, wherein high operating speed and smaller size are made possible by employing laminated structure of semiconductor elements without using the chip-on-chip configuration.

[MEANS FOR SOLVING PROBLEM] Semiconductor elements are mounted on both sides of a multi-layer wiring board having three-dimensional wiring based on inner via holes so that the semiconductor elements oppose each other via the multi-layer wiring board, and the electrodes of the semiconductor elements are connected with each other by means of the three-dimensional wiring of the multi-layer wiring board.

[SELECTED DRAWING] Fig. 1

Applicant Record

Identification No.: 000005821

1. Date of Registration: August 28, 1990 (newly recorded)

Address: 1006, Oaza Kadoma, Kadoma-shi, Osaka-fu

Name: Matsushita Electric Industrial Co., Ltd.